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Integrated Predicat d and Speculative Execution in the IMPACT EPIC Architecture (1998) (Make Corrections) (24 citations)

David I. August, Daniel A. Connors, Scott A. Mahlke, John W. Sias, Kevin M. Crozier, Ben-Chung Cheng, Patrick R. Eaton, Qudus B. Olaniran, Wen-mei W. Hwu

Proceedings of the 25th annual international symposium on Computer architecture

Abstract: Explicitly Parallel Instruction Computing (EPIC) architectures require the compiler to express program instruction level parallelism directly to the hardware. EPIC techniques which enable the compiler to represent control speculation, data dependence speculation, **and** predication have individually been shown to be very effective. However, these techniques have not been studied in combination with each other. This paper presents the IMPACT EPIC Architecture to address the issues involved in... (Update)

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Chen-Yong Cher **and** T. N. Vijaykumar - School Of Electrical (Correct)
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Pegasus: An Efficient Intermediate Representation - Budiu, Goldstein (2002) (Correct)

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D. I. August, D. A. Connors, S. A. Mahlke, J. W. Sias, K. M. Crozier, B. Cheng, P. R. Eaton, Q. B. Olaniran, **and** W. W. Hwu, "**Integrated Predicated and Speculative Execution** in the IMPACT EPIC Architecture," Proceedings of the 25th International Symposium on Computer Architecture, July 1998.
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title = "Integrated predicated and speculative execution in the {IMPACT {EPIC}}
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publisher = "IEEE Computer Society Press",
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126 Conversion of control dependence to data dependence (context) - Allen, Kennedy et al. - 1983
121 A VLIW architecture for a trace scheduling compiler (context) - Colwell, Nix et al. - 1987
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38 A comparison of full **and** partial **predicated execution** suppor.. - Mahlke, Hank et al. - 1995
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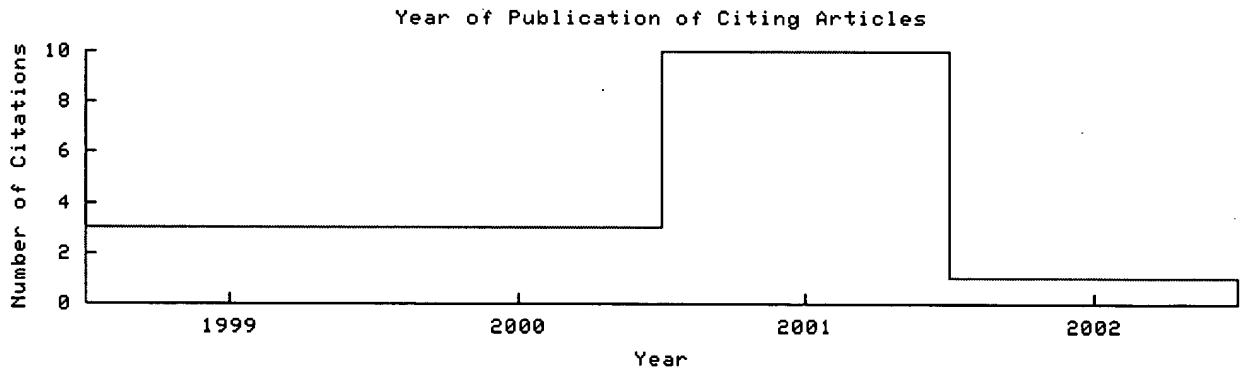

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George Almási , David Padua
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3 Performance monitoring: TEST: a tracer for extracting speculative threads 80%
Michael Chen , Kunle Olukotun
Proceedings of the international symposium on Code generation and optimization: feedback-directed and runtime optimization March 2003
Thread-level speculation (TLS) allows sequential programs to be arbitrarily decomposed into threads that can be safely executed in parallel. A key challenge for TLS processors is choosing thread decompositions that speedup the program. Current techniques for identifying decompositions have practical limitations in real systems. Traditional parallelizing compilers do not work effectively on most integer programs, and software profiling slows down program execution too much for real-time analysis. ...

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4 A compiler framework for speculative analysis and optimizations 80%

Jin Lin , Tong Chen , Wei-Chung Hsu , Pen-Chung Yew , Roy Dz-Ching Ju , Tin-Fook Ngai , Sun Chan

ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 2003 conference on Programming language design and implementation May 2003

Volume 38 Issue 5

Speculative execution, such as control speculation and data speculation, is an effective way to improve program performance. Using edge/path profile information or simple heuristic rules, existing compiler frameworks can adequately incorporate and exploit control speculation. However, very little has been done so far to allow existing compiler frameworks to incorporate and exploit data speculation effectively in various program transformations beyond instruction scheduling. This paper proposes a ...

5 Using dataflow analysis techniques to reduce ownership overhead in cache coherence protocols 80%

Jonas Skeppstedt , Per Stenström

ACM Transactions on Programming Languages and Systems (TOPLAS) November 1996

Volume 18 Issue 6

In this article, we explore the potential of classical dataflow analysis techniques in removing overhead in write-invalidate cache coherence protocols for shared-memory multiprocessors. We construct the compiler algorithms with varying degree of sophistication that detect loads followed by stores to the same address. Such loads are marked and constitute a hint to the cache to obtain an exclusive copy of the block so that the subsequent store does not introduce access penalties. The simplest ...

6 The Jrpm system for dynamically parallelizing Java programs 77%

Michael K. Chen , Kunle Olukotun

ACM SIGARCH Computer Architecture News , Proceedings of the 30th annual international symposium on Computer architecture May 2003

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We describe the Java runtime parallelizing machine (Jrpm), a complete system for parallelizing sequential programs automatically. Jrpm is based on a chip multiprocessor (CMP) with thread-level speculation (TLS) support. CMPs have low sharing and communication costs relative to traditional multiprocessors, and thread-level speculation (TLS) simplifies program parallelization by allowing us to parallelize optimistically without violating correct sequential program behavior. Using a Java virtual ma ...

7 Cool-Cache: A compiler-enabled energy efficient data caching framework for embedded/multimedia processors 77%

Osman S. Unsal , Raksit Ashok , Israel Koren , C. Mani Krishna , Csaba Andras Moritz

ACM Transactions on Embedded Computing Systems (TECS) August 2003

Volume 2 Issue 3

The unique characteristics of multimedia/embedded applications dictate media-sensitive architectural and compiler approaches to reduce the power consumption of the data cache. Our goal is exploring energy savings for embedded/multimedia workloads without sacrificing performance. Here, we present two complementary media-sensitive energy-saving techniques that leverage static information. While our first technique is applicable to existing architectures, in our second technique we adopt a more rad ...

8 Speculation: Compiler support for speculative multithreading architecture with probabilistic points-to analysis 77%

Peng-Sheng Chen , Ming-Yu Hung , Yuan-Shin Hwang , Roy Dz-Ching Ju , Jenq Kuen Lee

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Speculative multithreading (SpMT) architecture can exploit thread-level parallelism that cannot be identified statically. Speedup can be obtained by speculatively executing threads in parallel that are extracted from a sequential program. However, performance degradation might happen if the threads are highly dependent, since a recovery mechanism will be activated when a speculative thread executes incorrectly and such a recovery action usually incurs a very high penalty. Therefore, it is essent ...

9 How to solve the current memory access and data transfer bottlenecks: at the processor architecture or at the compiler level 77%

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David I. August , Daniel A. Connors , Scott A. Mahlke , John W. Sias , Kevin M. Crozier , Ben-Chung Cheng , Patrick R. Eaton , Qudus B. Olaniran , Wen-mei W. Hwu

ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture April 1998

Volume 26 Issue 3

Explicitly Parallel Instruction Computing (EPIC) architectures require the compiler to express program instruction level parallelism directly to the hardware. EPIC techniques which enable the compiler to represent control speculation, data dependence speculation, and predication have individually been shown to be very effective. However, these techniques have not been studied in combination with each other. This paper presents the IMPACT EPIC Architecture to address the issues involved in design ...

11 Evaluation of scheduling techniques on a SPARC-based VLIW testbed 77%

Seongbae Park , SangMin Shim , Soo-Mook Moon

Proceedings of the 30th annual ACM/IEEE international symposium on Microarchitecture December 1997

The performance of Very Long Instruction Word (VLIW) microprocessors depends on the close cooperation between the compiler and the architecture. This paper evaluates a set of important compilation techniques and related architectural features for VLIW machines. The evaluation is performed on a SPARC-based VLIW testbed where gcc-generated optimized SPARC code is scheduled into high-performance VLIW code. As a base scheduling compiler, we experiment with three core scheduling techniques including ...

12 Simple compiler algorithms to reduce ownership overhead in cache coherence protocols 77%

Jonas Skeppstedt , Per Stenström

Proceedings of the sixth internati nal conference on Architectural support f r programming languages and operating systems November 1994

Volume 29 , 28 Issue 11 , 5

We study in this paper the design and efficiency of compiler algorithms that remove

ownership overhead in shared-memory multiprocessors with write-invalidate protocols. These algorithms detect loads followed by stores to the same address. Such loads are marked and constitute a hint to the cache to obtain an exclusive copy of the block. We consider three algorithms where the first one focuses on load-store sequences within each basic block of code and the other two analyse the existence of l ...

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